WE CLAIM:

1. A carrier lock detector for use with a QPSK or low-level QAM system having a constellation of signal points identified by a plurality of I bits and Q bits respectively representing in-phase and quadrature components in a phasor diagram, the phasor diagram including a plurality of first areas centered on ideal signal points representing nominal states and a plurality of second areas adjacent to the first areas, the detector comprising:

a first counter responsive to a plurality of I bits and Q bits, the first counter producing a first output signal when a detected signal has I and Q components that map a signal point onto one of the first areas;

a second counter responsive to a plurality of I bits and Q bits, the second counter producing a second output signal when a detected signal has I and Q components that map a signal point onto one of the second areas; and

a logic device for computing a difference between the first output signal and the second output signal and for generating a carrier lock detection signal when the difference between the first output signal and the second output signal exceeds a threshold.

2. The carrier lock detector as claimed in claim 1, wherein the first areas are defined by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the second areas are defined by $\overline{Q_1 \oplus Q_2}\cdot\left(I_1\overline{I_2}\,\overline{I_3}+\overline{I_1}I_2I_3\right)+\left(\overline{I_1 \oplus I_2}\right)\cdot\left(Q_1\overline{Q_2}\,\overline{Q_3}+\overline{Q_1}Q_2Q_3\right)$.

3. The carrier lock detector as claimed in claim 1, wherein the first areas are defined by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the second areas are defined by $\left(\overline{I_1 \oplus I_2}\cdot\overline{Q_2 \oplus Q_3}\right)+\left(\overline{Q_1 \oplus Q_2}\cdot\overline{I_2 \oplus I_3}\right)$.

4. A coherent receiver with a carrier lock detector for use with a QPSK or low-level QAM system having a constellation of signal points identified by a plurality of I bits and Q bits respectively representing in-phase and quadrature components in a phasor diagram, the phasor diagram including a plurality of first areas centered on ideal signal points representing nominal states and a plurality of second areas adjacent to the first areas, comprising:

a first counter responsive to a plurality of I bits and Q bits, the first counter producing a first output signal when a detected signal has I and Q components that map a signal point onto one of the first areas;

a second counter responsive to a plurality of I bits and Q bits, the second counter producing a second output signal when a detected signal has I and Q components that map a signal point onto one of the second areas; and

a logic device for computing a difference between the first output signal and the second output signal and for generating a carrier lock detection signal when the difference between the first output signal and the second output signal exceeds a threshold.

5. The coherent receiver as claimed in claim 4, further comprising:

a local oscillator for generating a local signal having a local frequency different from that of a received signal;

a coupler for combining the incoming signal with the local signal to produce an intermediate signal;

a detector for detecting the intermediate signal;

a filter for filtering the intermediate signal;

a demodulator for separating the intermediate signal into analog I and Q components;

a first analog-to-digital converter for converting the analog I components into I bits; and

a second analog-to-digital converter for converting the analog Q components into Q bits.

6. The coherent receiver as claimed in claim 5 wherein the first analog-to-digital converter is a 3-bit analog-to-digital converter for decoding I bits designated as I_1, I_2, I_3 where I_1 is the most significant I bit; and the second analog-to-digital converter is a 3-bit analog-to-digital converter for decoding Q bits designated as Q_1, Q_2, Q_3, where Q_1 is the most significant Q bit.

7. The coherent receiver as claimed in claim 6, wherein the first areas are defined by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the

second areas are defined by $\overline{Q_1 \oplus Q_2} \cdot \left(I_1 \overline{I_2} \overline{I_3} + \overline{I_1} I_2 I_3\right) + \left(\overline{I_1 \oplus I_2}\right) \cdot \left(Q_1 \overline{Q_2} \overline{Q_3} + \overline{Q_1} Q_2 Q_3\right)$.

8. The coherent receiver as claimed in claim 6, wherein the first areas are defined by $(I_2 \oplus I_3) \cdot (Q_2 \oplus Q_3)$ and the second areas are defined by $\left(\overline{I_1 \oplus I_2} \cdot \overline{Q_2 \oplus Q_3}\right) + \left(\overline{Q_1 \oplus Q_2} \cdot \overline{I_2 \oplus I_3}\right)$.

9. The coherent receiver as claimed in claim 7 wherein the local oscillator comprises a laser.

10. The coherent receiver as claimed in claim 9 wherein the detector comprises a photodiode.

11. The coherent receiver as claimed in claim 10 wherein the filter comprises a low-pass filter and an AC coupling.

12. The coherent receiver as claimed in claim 11 wherein the coupler is an optical hybrid.

13. The coherent receiver as claimed in claim 8 wherein the local oscillator comprises a laser.

14. The coherent receiver as claimed in claim 13 wherein the detector comprises a photodiode diode.

15. The coherent receiver as claimed in claim 14 wherein the filter comprises a low-pass filter and an AC coupling.

16. The coherent receiver as claimed in claim 15 wherein the coupler comprises an optical hybrid.

17. A method of detecting carrier lock in a QPSK or low-level QAM system having a constellation of signal points identified by a plurality of I bits and Q bits respectively representing in-phase and quadrature components in a phasor diagram, the phasor diagram including a plurality of first areas centered on ideal signal points representing nominal states and a plurality of second areas adjacent to the first areas, the method comprising the steps of:

monitoring a plurality of less significant I and Q bits;

generating a first signal when a detected received signal has I and Q components that map onto one of the first areas;

generating a second signal when the detected received signal has I and Q components that map onto one of the second areas;

computing a difference between the first signal and the second signal;

comparing the difference with a threshold value; and

generating a carrier lock detection signal when the difference exceeds the threshold.

18. The method as claimed in claim 17 further comprising the step of defining the first areas by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the second areas by $\overline{Q_1 \oplus Q_2}\cdot\left(I_1\overline{I_2}\,\overline{I_3} + \overline{I_1}I_2I_3\right) + \left(\overline{I_1 \oplus I_2}\right)\cdot\left(Q_1\overline{Q_2}\,\overline{Q_3} + \overline{Q_1}Q_2Q_3\right)$.

19. The method as claimed in claim 18 further comprising a step of defining the first areas by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the second areas by $\left(\overline{I_1 \oplus I_2}\cdot\overline{Q_2 \oplus Q_3}\right) + \left(\overline{Q_1 \oplus Q_2}\cdot\overline{I_2 \oplus I_3}\right)$.

20. The method as claimed in claim 17 wherein the steps of generating a first signal and generating a second signal are accomplished using a device selected from the group consisting of a RAM and a lookup table.